AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A driving circuit for a flat panel display, the circuit comprising:

a latch unit to which a control signal is applied from a shift register to sample at least one digital picture signal and to store the digital picture signal, the latch unit simultaneously outputting the sampled picture signal by a line pass signal; and

a voltage to current converting unit supplying current of a plurality of levels to a data line of the display panel according to logical combinations of the sampled picture signal from the latch unit, using a current mirror method, wherein the voltage to current converting unit includes a plurality of poly-crystalline switching units formed on the display panel.

2. (Previously Presented) The circuit of claim 1, wherein the latch unit comprises:

a first latch unit being applied the control signal from the shift register to sample and store the digital picture signal having a plurality of bit numbers; and

a second latch unit outputting the digital picture signal sampled in the first latch unit simultaneously according to the line pass signal.

3. (Original) The circuit of claim 1, wherein the shift register, the latch unit and the voltage to current converting unit are formed in the display panel.

4. (Original) The circuit of claim 1, wherein the display panel is an organic electroluminescence display panel.

5. (Currently Amended) ~~The circuit of claim 1~~ A driving circuit for a flat panel display, the circuit comprising:

a latch unit to which a control signal is applied from a shift register to sample at least one digital picture signal and to store the digital picture signal, the latch unit simultaneously outputting the sampled picture signal by a line pass signal; and

a voltage to current converting unit supplying current of a plurality of levels to a data line of the display panel according to logical combinations of the sampled picture signal from the latch unit, using a current mirror method,

wherein the voltage to current converting unit comprises:

a first switching unit for controlling a flow of a reference current by an enable signal;

a second switching unit connected to the first switching unit for controlling the flow of the reference current by the enable signal; and

a plurality of switching units for controlling switching of ~~the~~a plurality of current paths by being applied the sampled picture signal having a plurality of bit numbers independently.

6. (Previously Presented) The circuit of claim 18, wherein the first NMOS transistor and the plurality of NMOS transistors are poly-crystalline silicon thin film transistors (TFTs).

7. (Original) The circuit of claim 5, wherein the first switching unit, second switching unit and the plurality of switching units comprise NMOS transistors.

8. (Original) The circuit of claim 7, wherein each NMOS transistor is a poly-crystalline silicon TFT.

9. (Original) The circuit of claim 5 further comprising a capacitor connected between the second switching unit and ground for charging the reference current.

10. (Previously Presented) The circuit of claim 18, wherein the plurality of NMOS transistors includes an NMOS transistor for resetting the gate electrodes of the first NMOS transistor which forms the reference path and of the plurality of NMOS transistors which form the plurality of current paths in a parallel direction to ground potential by a reset signal.

11. (Previously Presented) The circuit of claim 16, wherein the plurality of current paths are formed to be the same as bit numbers of the sampled picture signal.

12. (Previously Presented) The circuit of claim 16, wherein the plurality of current paths are formed to be the same as a number of logical combinations of bits of the sampled picture signal.

13. (Previously Presented) The circuit of claim 18, wherein the first NMOS transistor is formed to have a ratio of channel width/length differently from those of the plurality of NMOS transistors.

14. (Original) The circuit of claim 13, wherein the ratios of channel widths/lengths of the plural NMOS transistors are made to be different from those of each other.

15. (Original) The circuit of claim 13, wherein the ratios of channel widths/lengths of the plurality NMOS transistors are made to be the same as each other.

16. (Previously Presented) The circuit of claim 1, wherein the voltage to current converting unit includes a current mirror structure with a plurality of current paths.

17. (Previously Presented) The circuit of claim 16, wherein the current mirror structure receives a reference current and supplies the current of the plurality of levels selectively from at least one of the plurality of current paths according to the logical combinations of the sampled picture signal.

18. (Previously Presented) The circuit of claim 5, wherein the voltage to current converting unit further includes:

a first NMOS transistor for forming a reference path on which the reference current flows between the first switching unit and ground by being applied the reference current on a gate electrode thereof; and

a plurality of NMOS transistors not including the first NMOS transistor for forming the plurality of current paths in a parallel direction between the data line and the ground of the

display panel according to the sampled picture signal having a plurality of bit numbers by being applied the reference current on respective gate electrodes thereof.

19. (Currently Amended) A flat panel display, comprising:

a substrate;

a plurality of pixel units located on the substrate; and

a data driving circuit located on the same substrate, the data driving circuit including a plurality of current paths, the data driving circuit supplying current of a plurality of levels to at least one of the plurality of pixel units by providing the current from at least one of the plurality of current paths, wherein the current mirror paths are formed on the substrate.

20. (Previously Presented) The flat panel display of claim 19, wherein the data driving circuit includes a current mirror structure on the same substrate, the current mirror structure receiving a reference current to provide the current from the at least one of the plurality of current paths based upon logical combinations of bits of a digital picture signal.

21. (Previously Presented) The flat panel display of claim 19, wherein the flat panel display is an organic electroluminescence display.